REMARKS

Claims 1-10, 19-34, and 37-40 are pending in the application.

Claims 1-10 and 19-34 stand rejected.

Claims 1, 19, and 27 have been amended. Claims 37-40 have been added. Support for the amendments and added claims can be found, at least, in canceled claims 11-18 as well as in FIGs. 5A-5B and the accompany description.

Rejection of Claims under 35 U.S.C. §102

Claims 1, 3, 5-7, 9-10, 19, 21, 23-24, 26-27, 29, 31-32, and 35 are rejected under 35 U.S.C. §102(e) as being anticipated by Li et al. (U.S. Patent No. 6,721,929) (hereinafter referred to as "Li"). Applicant respectfully traverses this rejection.

The sections of Li identified in the Office Action do not anticipate, teach, or suggest "calculating an effective capacitance of the interconnect model to be inversely proportional to a voltage at the driving point node of the interconnect model, wherein the calculating the effective capacitance of the interconnect model comprises scaling one or more capacitances by a ratio of a voltage across the one or more capacitances to the voltage at the driving point node," as recited in amended claim 1.

Li states:

> "In one embodiment, the RC network is reduced to a network response function (e.g., transfer function) representation, G(s), for the corresponding RC network. Also, the impedance of the RC network at the driving point, Z(s), is also computed... The new current, I_d(T), for the new time instance, T, is applied to drive the RC network (block 720, FIG. 7). From the RC network impedance at the driving point, Z(s), the V_d, for time T, is computed using the Id for time T as follows:
>
> $Vd(s) = I(s) * Z(s)$
>
> (block 740, FIG. 7). From the new voltage, V_d, for the time instance at time T, the process calculates an effective capacitance, C_{eff}(T), using the current, I_d(T), the voltage V_d(T) and the time of the instance, T (block 750, FIG. 7). Specifically, the effective capacitance, C_{eff}(T), is calculated from the expression:
>
> $Id(T)=Vd(T)*Ceff(T)/T$
>
> $Ceff(T)= Id(T)*T/Vd(T)$
>
> The new effective capacitance C_{eff}(T), combined with the voltage, V_d, at the driving point, affects the new effective driving current... The process is repeated using the new current to drive the RC network to obtain a new voltage and a new effective capacitance." Li, col. 7, lines 2-42.

Thus, Li teaches an iterative technique for calculating effective capacitance based on driving current and driving point voltage. Clearly, this technique neither teaches nor suggests calculating the effective capacitance of the interconnect model comprises scaling one or more capacitances by a ratio of a voltage across the one or more capacitances to the voltage at the driving point node. Accordingly, claim 1 is patentable over the cited art for at least the foregoing reason. Claims 3, 5-7, 9-10, and 38-40, which depend from claim 1, are also patentable over the cited art for at least this reason. Claims 19, 21, 23-24, 26-27, 29, 31-32, and 35 are patentable over the cited art for similar reasons.

Claims 1-8, 10, 19-25, and 27-33 are rejected under 35 U.S.C. §102(e) as being anticipated by Puri et al. (U.S. Patent No. 6,601,223) (hereinafter referred to as "Puri"). Applicant respectfully traverses this rejection.

The sections of Puri identified in the Office Action fail to anticipate, teach, or suggest "calculating an effective capacitance of the interconnect model to be inversely proportional to a voltage at the driving point node of the interconnect model," as recited in claim 1. The Office Action refers to FIGs. 1-3, 5-6, and cols. 5-11 of Puri as teaching this feature of claim 1. Applicant's representative is unable to find any teachings in the cited portions of Puri that suggest "calculating an effective capacitance... to be inversely proportional to a voltage at the driving point node." At best, Puri describes an iterative technique for calculating effective capacitance that involves the following steps:

> "1. Initialize the effective capacitance of each RC tree node i (i.e., $C_{eff}(i)$) with the sum of all downstream capacitances (Step 610).
>
> 2. Initialize the delay on each RC-tree segment with corresponding Elmore delays (Step 620).
>
> 3. Compute the slew at the source of RC-tree, i.e., output of driver with last computed C_{eff}(source) (Step 630).
>
> 4. Calculate the slews of each RC tree segment, by moving outward from the source node towards the sinks (Step 640) ...
>
> 5. Recalculate the effective capacitance of each node starting from the sinks and traversing backwards towards the source (Step 650). The effective capacitance is calculated by using the capacitance shielding factor as derived above.
>
> 6. Update the Elmore delay values of each RC-tree segment using new effective capacitance values (step 660).

> 7. Recalculate the driver output slew (Step 670) using the effective load capacitance determined in the previous backward propagation pass (i.e., Step 650). If driver slew did not converge within a specified threshold of previous slew (as determined in Step 680), iterate over step 4 to step 7 again until the slew at the drive output converges (repeat Steps 640-680)." Puri, col. 7, line 38-col. 8, line 21.

Puri's technique for calculating effective capacitance does not involve calculating an effective capacitance of the interconnect model to be inversely proportional to a voltage at the driving point node of the interconnect model. Accordingly, claim 1 is patentable over the cited art. Claims 2-8, 10, 19-25, 27-33, and 37-40 are patentable for similar reasons.

Additionally, Applicant notes that, under 37 C.F.R. §1.104(c)(2), "The examiner must cite the best references at his or her command. When a reference is complex or shows or describes inventions other than that claimed by the applicant, the particular part relied on must be designated as nearly as practicable." Applicant respectfully request that the Examiner more clearly point out which portion of FIGs. 1-3, 5-6, and cols. 5-11 of Puri is being relied upon in the rejection of claim 1.

Claims 1, 3-10, 19, 21-27, and 29-34 are rejected under 35 U.S.C. §102(b) as being anticipated by Muddu (U.S. Patent No. 6,314,546) (hereinafter referred to as "Muddu"). Applicant respectfully traverses this rejection.

The sections of Muddu identified in the Office Action fail to anticipate, teach, or suggest "calculating an effective capacitance of the interconnect model to be inversely proportional to a voltage at the driving point node of the interconnect model," as recited in claim 1. Muddu states that $C_{eff} = C_{step} + (C_{tot} - C_{step}) / (1 + D_{LD}/D_{NL}$. Muddu also states that the foregoing relationship implies that $C_{eff} = C_{step}$ if $D_{LD}/D_{NL} >> 1$, and $C_{eff} = C_{tot}$ if $D_{LD}/D_{NL} << 1$, where D_{NL} is the intrinsic gate delay and D_{LD} is the intrinsic gate load delay. Muddu, col. 9, lines 63-64 and col. 10, lines 3-16. This neither teaches nor suggests calculating an effective capacitance of the interconnect model to be inversely proportional to a voltage at the driving point node of the interconnect model, and thus claim 1 is patentable over the cited art. Claims 3-10, 19, 21-27, 29-34, and 37-40 are patentable over the cited art for similar reasons.

CONCLUSION

In view of the amendments and remarks set forth herein, the application is believed to be in condition for allowance and a notice to that effect is solicited. Nonetheless, should any issues remain that might be subject to resolution through a telephonic interview, the Examiner is invited to telephone the undersigned at 512-439-5087.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on **March 15, 2005**.

Brenna A Brock 3-15-2005
Attorney for Applicants Date of Signature

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